GP2815/B
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IR-1529 (2-1979)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	New York, New York
Chuan Cheah et al.	Date: March 23, 1999
Serial No.: 09/225,153	Group Art Unit: --
Filed: January 4, 1999	Examiner: --
For: SEMICONDUCTOR PACKAGE	

Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION TO MAKE NEW APPLICATION
SPECIAL UNDER MPEP §708.02 VIII

Sir:

1. Petition:

Applicant hereby petitions to make the above-identified application special under MPEP §708.02, VIII. The application has not yet been examined.

2. Claims:

(a) All the claims in this case are directed to a single invention.

(b) If the Office determines that all the claims presented are not obviously directed to a single invention, applicants will make an election without traverse as a prerequisite to the grant of special status.

29 June 99

3. Search:

A search was made in the U.S. Patent and Trademark Office search room. The search was directed to electronic packages in class 257, subclasses 688, 689, 690, 691, 692, and 696, which cover the general subject matter of the present invention.

The patents uncovered and deemed most clearly related to the subject matter encompassed by the claims are listed below and on the attached Form PTO-1449.

4. Copies of References:

A copy of each of the following patents located in the search deemed most clearly related to the subject matter encompassed by the claims is as follows (copies submitted herewith):

U.S. Patent No.	Inventor	Date
5,119,169	Kozono et al.	June 2, 1992
5,145,800	Arai et al.	September 8, 1992
5,461,255	Chan et al.	October 24, 1995
5,498,907	Tumpey et al.	March 12, 1996
5,550,401	Maeda	August 27, 1996
5,559,373	Applebaum	September 24, 1996
5,631,476	Ferla et al.	May 20, 1997
5,637,922	Fillion et al.	June 10, 1997

5. Discussion of References:

U.S. Patent No. 5,498,907 to Tumpey discloses an interconnection arrangement for power semiconductor switching devices in which the devices are arranged in an elliptical pattern to provide a circuit module 14. The Tumpey patent does not disclose or suggest a power semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,559,373 to Applebaum discloses a one piece contact member 14 having a frame portion 18 and a connection portion 20 disposed atop a diode 8. The connection portion 20 is bonded to the anode surface of the diode. The Applebaum patent does not disclose or suggest a semiconductor

package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package.

U.S. Patent No. 5,637,922 to Fillion discloses radio frequency power semiconductor devices employing a high density interconnect. In particular, the Fillion patent discloses a power device component package including a substrate, a power device component and a dielectric layer overlying at least a portion of the component. The package includes a pattern of electrical conductors extending through selected vias. The Fillion patent does not disclose or suggest a power semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,461,255 to Chan discloses a multi-layered leadframe assembly for integrated circuits. A plurality of bond pads are disposed along the center line of the leadframe. Selective leads of the main leadframe are electrically interconnected with respective leads of a bus. The Chan patent does not disclose or suggest a semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,145,800 to Arai discloses a method of wiring a power supply to a large-scale integrated circuit. A plurality of longitudinally extending power supply wires and transversely extending power supply wires are disposed across an integrated circuit chip to define a power supply grid. The Arai patent does not disclose or suggest a semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial

part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,119,169 to Kozono discloses a semiconductor integrated circuit device including a semiconductor substrate, a first auxiliary power source, and a second auxiliary power source arranged in a lattus form. The Kozono patent does not disclose or suggest a semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,550,401 to Maeda discloses a lead on chip semiconductor device including multiple bonding pads connected to a bonding terminal of a leadframe. Bonding terminal portions for multiple signal lines of the leadframe and the multiple power source lines are bonded via an electrical insulator. Power source lines extend in a three dimensional crossed configuration and are electrically insulated from the signal line. The Maeda patent does not disclose or suggest a semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a terminal of the package as recited in the independent claims of the present invention.

U.S. Patent No. 5,631,476 to Ferla discloses a MOS-technology power package assembly including a semiconductor device having a plurality of contact pads thereon. A plurality of bonding wires couple respective pads to terminals of the package. The Ferla patent does not disclose or suggest a semiconductor package including a power MOSFET coupled to a bottom plate of a leadframe, a copper plate coupled to and spanning a substantial part of the source connection of the MOSFET, and a beam portion for coupling the copper plate to a

terminal of the package as recited in the independent claims of the present invention.

6. **Fee:**

Our check No. 83277 in the amount of $130.00 as required by 37 C.F.R. §1.17(i) is attached.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 23, 1999

Samuel H. Weiner

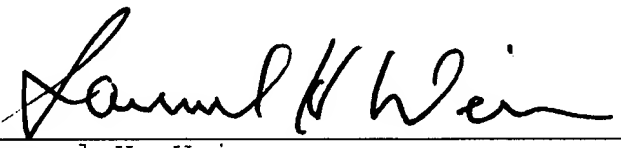
Name of applicant, assignee or Registered Representative

Signature

March 23, 1999

Date of Signature

Respectfully submitted,



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SHW/MBD:dmt

APPLICANT'S ART CITATION (Use several sheets if necessary)	Application 09/225,153	OFGS File No. IR-1529 (2-1979)
	Applicant Chuan Cheah et al.	
	Filing Date January 4, 1999	Group Art Unit

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date If Appropriate
	5 1 1 9 1 6 9	6/2/92	Kozono et al.			
	5 1 4 5 8 0 0	9/8/92	Arai et al.			
	5 4 6 1 2 5 5	10/24/95	Chan et al.			
	5 4 9 8 9 0 7	3/12/96	Tumpey et al.			
	5 5 5 0 4 0 1	8/27/96	Maeda			
	5 5 5 9 3 7 3	9/24/96	Applebaum			
	5 6 3 1 4 7 6	5/20/97	Ferla et al.			
	5 6 3 7 9 2 2	6/10/97	Fillion et al.			

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Sub-class	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.